



VERIFICATION OF CONCURRENT PROGRAMS ASSISTED BY CODE AND SPECIFICATION TRANSFORMATION

PHD THESIS DEFENCE

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December 6th, 2016







Code and Specification Transformation

Weak Memory Models

Conclusion, Future Work

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- 2 Code and Specification Transformation
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Weak Memory Models

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Weak Memory Models

Conclusion, Future Work

Complex software

- Software is composed of millions of lines of code
- More multi-core architectures
- More concurrent programs

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 0xA1015000	
 0x7000BAD0	
 0x8F000000	
 0x12345678	
0x00000000	
 OxFFFFFFFF	

How can we ensure the validity of our software ?

Code and Specification Transformation

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Existing Methods

Most commonly used

Program testing

Formal Methods

- Abstract interpretation
- Model-checking
- Theorem proving

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Concurrent Programs Logics

Assuming sequentially consistent memory model

- HOARE 1975. Critical sections, abstract from time
- OWICKI-GRIES 1976. Resource invariant, ghost variables
- Rely-Guarantee, JONES 1983. Interferences
- Concurrent Separation Logic, O'HEARN et al 2007
- Combination of RG and CSL, VAFEIADIS et al 2007

Assuming weak memory models

- Relaxed separation logic, VAFEIADIS et al 2013
- Ghost, Procotols and Separation, VAFEIADIS et al 2014

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Existing Verification Tools

Concurrent C code verification

- VCC (Owicki-Gries + ~ Rely Guarantee + Ownership)
- Verifast (Separation logic)

FRAMA-C

- C code analysis
- Modular architecture based on plugins
- Most analyses do not handle concurrency





Contribution

Code and Specification Transformation

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Code and specification transformation

Transform a concurrent code into a (simulating) sequential one

- Experimented on a use case
- Automated in a FRAMA-C plugin
- Proved sound

Weak memory models

A constraint based solver for weak memory behaviors

- Generate all candidate executions of a program
- Determine for each one if it is allowed by a given model

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Overview

Case study: Micro-kernel code CONC2SEQ: Automated method as a FRAMA-C plugin Soundness proof

3 Weak Memory Models



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Specifications

Original Code (Concurrent)

Requirements

- Equivalence of code must be proved
- Do not alter specification meaning
- Added specifications must always be automatically proved

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Program Verification

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Code transformation

- Each local variable becomes a simulating array
- Each instruction becomes a function
- All functions are interleaved to simulate concurrency

We suppose an interleaving semantics \Rightarrow SC memory model

Specifications transformation

- Invariants are simulating functions pre/post conditions
- Each variable is replaced by its simulation counterpart

Code and Specification Transformation

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Case study – Micro-kernel code

- Anaxagoros Microkernel Virtual Memory Subsystem
 - Manages memory pages
 - Organized as hierarchy
 - Counts mappings to pages
- We want to verify the function used to update page tables
 - For any page, the indicated number of mappings must be greater or equal to the reality



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Case study – Verification results

For atomic low-level functions

- ACSL specifications
- Proof with FRAMA-C and WP

For the page update function (concurrent)

- Specification and proof for sequential version
- Simulation of concurrent executions
- Weakening of the specification and proof:
 - Mostly automatic with FRAMA-C and WP
 - Auxiliary lemmas proved with Coq

Code and Specification Transformation

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Original Code

Case study – Simulation

```
#define NOF 2048
#define MAX 256
uint mappings[NOF];
int set_entry(uint fn, uint idx, uint new){
    uint c_n = mappings[new];
    if(c_n >= MAX) return 1;
    if(!CAS(&mappings[new], c_n, c_n+1))
        return 1;
    page_t p = get_frame(fn);
    uint old = atomic_exchange(&p[idx], new);
    if(!old) return 0;
    fetch_and_sub(&mappings[old], 1);
    return 0;
}
```

Simulating Code

```
#define THD 16
```

```
uint pct[THD];
```

```
uint fn [THD];
uint idx[THD];
uint new[THD];
uint c_n[THD];
uint old[THD];
```

```
//@ghost uint ref[THD]
```

. . .

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    return 1;
    page_t p = get_frame(fn);
    uint old = atomic_exchange(&p[idx], new);
    if(!old) return 0;
    fetch_and_sub(&mappings[old], 1);
    return 0;
```

Simulating Code

```
void gen_args(uint th){
  fn[th] = random_page();
  idx[th] = random_idx();
  new[th] = random_page();
  pct[th] = 1;
}
```

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Original Code

Case study – Simulation

```
#define NOE 2048
#define MAX 256
uint mappings[NOF];
                                               void read map new(uint th){
int set entry(uint fn, uint idx, uint new){
                                                 c n[th] = mappings[new[th]];
  uint c n = mappings[new];
                                                 pct[th] = 2:
 if(c n \ge MAX) return 1;
                                               }
  if(!CAS(&mappings[new], c n, c n+1))
    return 1;
  page t p = get frame(fn);
 uint old = atomic exchange(&p[idx], new);
  if(!old) return 0:
  fetch and sub(&mappings[old], 1);
  return 0;
```

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Case study – Simulation

```
#define NOF 2048
#define MAX 256
uint mappings[NOF];
int set_entry(uint fn, uint idx, uint new){
    uint c_n = mappings[new];
    if(c_n >= MAX) return 1;
    if(!CAS(&mappings[new], c_n, c_n+1))
        return 1;
    page_t p = get_frame(fn);
    uint old = atomic_exchange(&p[idx], new);
    if(!old) return 0;
    fetch_and_sub(&mappings[old], 1);
    return 0;
}
```

Simulating Code

```
. . .
```

```
void interleaving(){
  while(true){
    uint th = choose a thread();
```

```
switch(pct[th]){
    case 0 : gen_args(th); break;
    case 1 : read_map_new(th); break;
    case 2 : test_map_new(th); break;
    case 3 : cas_map_new(th); break;
    case 4 : exch_entry(th); break;
    case 6 : test_old(th); break;
  }
```

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Case study – Benefits and Limitations

Verification results

- Using FRAMA-C with WP
- Mostly automatic thanks to SMT solvers (CVC4, Z3)
- Completed by interactive proof using COQ

Limitations

- Most of the work could have been done automatically
- Known fixed-size arrays : fixed number of threads
- Limited scaling expected

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CONC2SEQ – Features

CONC2SEQ role

- Perform code transformation
- Adapt specifications

Supported

- Most C instructions
- Thread local variables
- Atomic operations (stdatomic.h)
- Atomic blocks of code
- Global invariants

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CONC2SEQ – Code transformation: variables

Generated Code

Original Code

```
int global;
int th_v thread_local;
void foo(){
   int v;
}
```

int* pct; int global; int* tl_th_v; int* foo_v;

/*@ axiomatic Validity_of_sim_vars {
 predicate simulation{L} reads <sim ptrs>;

axiom all_simulations_separated{L}:
ssimulating>variables separation
\separated(<memory blocks/globals>);

axiom pct_is_valid{L}: simulation ==> (\forall integer i valid th(i))==> (\simulating variables validity (\valid(\ac(pct,L)+j)); //... } */

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CONC2SEQ - Code transformation: atomic instructions

Original Code

```
void foo(){
    int v;
    th_v = atomic_load(&global);
```

```
/*@ atomic \true; */{
    v = 42;
    global += v;
}
```

Generated Code

```
void foo_Call_1(uint th){
   tl_th_v[th] = atomic_load(&global);
   pct[th] = 2;
}
```

```
void foo_Atomic_2(uint th){
  foo_v[th] = 42;
  global += foo_v[th];
  pct[th] = 3;
}
```

CONC2SEQ - ACSL fold

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New ACSL built-in to talk about threads

A logic fold operation on the value of a variable for all threads

- Generate an axiomatic definition for each usage ...
- ... according to provided types and logic function.

Idea

```
thread_reduction(func, v, init)
⇔
func(sim_v[0], func(..., func(sim_v[NTH], init)))
```

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Soundness proof – Simplified language

mth	::=	m(list x)block	<i>m</i> ∈ <i>Names</i>
main	::=	m(list e)	
С	::=	x := e	local assignment
		x[y] := e	memory store
		x := y[e]	memory load
		while e do block	
		if e then block else block	
		m(list e)	call
		atomic block	
V	::=	n I b	$n \in \mathbb{Z}, l \in \mathbb{L}, b \in \mathbb{B},$
е	::=	$v \mid x \mid op(\bar{e})$	$x \in \mathcal{X}$

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Soundness proof – Definitions: States and Traces

States

local environments heaps global state (seq) global state (||)

$$\begin{split} & \boldsymbol{P} = \{ \boldsymbol{\rho} : \mathcal{X} \rightharpoonup \mathcal{V} \} \\ & \boldsymbol{\Sigma} = \{ \boldsymbol{\sigma} : \mathbb{L} \rightharpoonup \mathbb{N} \rightharpoonup \mathcal{V} \} \\ & \boldsymbol{\gamma}_{seq} : \boldsymbol{\Sigma} \times \overline{Names \times P \times \mathcal{C}} \\ & \boldsymbol{\gamma}_{\parallel} : \boldsymbol{\Sigma} \times (\mathbb{T} \rightarrow \overline{Names \times P \times \mathcal{C}}) \end{split}$$

Traces

Actions:

a ::= τ | call m | return m | read l n v | write l n v

🔳 atomic *a**

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Soundness proof – Hypotheses

Memory

- Statically allocated
- Does not initially contain addresses

Forbidden actions

- Nested atomic blocks
- Thread spawning
- Recursive functions

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Soundness proof – Function call/return

New simulating memory blocks

- For each function we add an address *from* in the heap
- It indicates the next instruction to perform in the caller

Call/Return simulation

- Call simulation updates from for the executed thread
- Return simulation puts the program counter to this value

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Soundness proof – Equivalences

State equivalence

$$\sigma_{\textit{sim}} = \sigma_{\parallel} \sqcup \sigma_{\textit{sim},\mathcal{X}}$$

 $\sigma_{sim,\mathcal{X}}$ correctly represents every local environment

• $\sigma_{sim,\mathcal{X}}$ correctly models every stacks

Trace equivalence

Forall action (t, a), we have a list of actions (write ptid 0 t) :: I, where:

I = [] if
$$a$$
 is τ

- I = [a] if *a* is a memory access
- *I* = [call *m*] if *a* is a call/return and *m* is its simulation
- *I* is the list of actions of *a*, if *a* is an atomic block action.

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Soundness proof – Main result

Theorem

Forall (safe) p_{\parallel} , p_s its simulation, from states $\gamma_{\parallel,init}$ and $\gamma_{s,init}$

- **by** simulation initialization, we reach $\gamma_{s,0}$ equivalent to $\gamma_{\parallel,init}$
- forall γ_s reachable from $\gamma_{s,0}$ with a trace t_s , there exists γ_{\parallel} reachable from $\gamma_{\parallel,init}$ with a trace t_{\parallel} equivalent to t_s .
- forall γ_{\parallel} reachable from $\gamma_{\parallel,init}$ with a trace t_{\parallel} , there exists γ_s reachable from $\gamma_{s,0}$ with a trace t_s equivalent to t_{\parallel} .

Proof ideas

- Sequential actions are deterministic, their translation too
- Thread selection: just choose the same thread

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Formalization – Toward a COQ proof

Implemented up to known

- Language and semantics
- Transformation function

Next steps

- Write equivalence in COQ
- Perform the COQ proof

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Sequential consistency vs. Weak memory models A solver for weak memory behaviors Results



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Sequential Consistency (Lamport 1979)

A simple program

Thread 0	Thread 1
x := 1;	y := 1;
$r_0 := y;$	$r_1 := x;$

Possible results :

- $\blacksquare r_0 = 1 \wedge r_1 = 1$
- $\mathbf{I} \mathbf{r}_0 = \mathbf{0} \wedge \mathbf{r}_1 = \mathbf{1}$

$$\mathbf{r}_0 = \mathbf{1} \wedge \mathbf{r}_1 = \mathbf{0}$$

Impossible result :

$$\mathbf{I} \mathbf{r}_0 = \mathbf{0} \wedge \mathbf{r}_1 = \mathbf{0}$$

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Existing dedicated tools

Herding cats (Alglave et al. 2014)

Generic framework for weak behaviors

- Written in OCAML
- Provides a language to specify memory models

JMMSolve (Schrijvers 2004) based on CCMM (Saraswat 2004)

Program executions under Java Memory Model

- Based on Concurrent Constraint-based Memory Machines
- Written using Constraint Handling Rules (CHR)

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Prolog

Prolog and CHR

Declarative language for logic programming

Constraint Handling Rules

Declarative language for constraint programming

- Maintains a store of constraints (~ terms)
- Handled by rules that will add or remove constraints

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Goals of our solver

To identify allowed executions

- For a given parallel program
- According to a given memory model

Additional goals

- Possibility to add new memory models
- Support of specific instructions

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Chosen approach

Generate all candidate executions

An execution is represented by ordering relations :

- For each location *I*, a total ordering of every store to *I* (CO)
- For each load, a store having written the read value (RF)
- We combine all permutations of CO/RF using backtracking

Filter out forbidden executions

- Apply model rules to deduce more ordering relations
- Incoherent execution: an action must happen before itself (which means that some relations exhibit a cycle)

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Express and derive relations with CHR

Ordering relations vs. CHR constraints



CHR rules to derive new relations :

- $rf(ST, LD), co(ST, ST2) \Rightarrow fr(LD, ST2).$
- Ifr(LD, ST2), co(ST2, ST3) ⇒ fr(LD, ST3).



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Express and derive relations with CHR

Ordering relations vs. CHR constraints

Relation	CHR constraint
$x := 0 \xrightarrow{CO} x := 1$	co(x := 0, x := 1)
$x := 2 \xrightarrow{RF} r := x$	rf(x := 2, r := x(2))

CHR rules to derive new relations :

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CHR rules to derive new relations :

- rf(ST,LD), co(ST,ST2) ⇒ fr(LD,ST2).
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Definition of a model : SC

Definition of a model

Define a new relation as the union of maintained relations

```
co(I,J) ==> sc(I,J).
rf(I,J) ==> sc(I,J).
fr(I,J) ==> sc(I,J).
po(I,J) ==> sc(I,J).
```



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```



Program Verification

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Available Models

- SC, TSO, PSO and ARM (Almost finished)
- Easy to extend new memory models

Program samples from Herd

Our solver has been tested on 18 examples of litmus programs

- Message passing,
- Basic uniproc relations,
- · · · ·

We observe the same results found by Herd.

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Performance tests

Multiple message passing

Example	Model	#exec	Herd	CHR Solver
MP3	Generic	147 436	1.2s	3.3s
	PSO	2 258	3.8s	6.4s
	TSO	800	4.1s	3.2s
	SC	678	5.5s	3.3s
MP4	Generic	255 000 000	1405s	> 1h
	PSO	516030	> 1h	2796s
	TSO	96 498	> 1h	752s
	SC	81 882	> 1h	747s

Early pruning makes the solver efficient for "long" programs. Our solver was not so hard to implement.

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Contribution

A method for the verification of concurrent code

- Under sequentially consistent memory model
- Based on code and specification transformation

Our method is

- Successfully applied on a part of a microkernel [FMICS 2015]
- Now automated in a Frama-C plugin [SCAM 2016]
- Proved sound on paper, to be proved using COQ.
- A CHR based solver for weak memory behaviors [CSTVA 2016]
 - It can identify executions allowed by a memory model
 - It has interesting performances on "big" programs

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Future Work

Make the plugin compatible with other plugins

- Currently only WP is supported
- Determine critical features

Make further experiments

- Integrate function call in CONC2SEQ
- Analyze more case studies

Add new features to our CHR solver

- Complete ARM
- Arithmetic and branching instructions

Combine CONC2SEQ and our CHR solver

Validate sequentialy consistent behavior using the solver

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Publications

Allan Blanchard, Nikolai Kosmatov, Matthieu Lemerre, and Frédéric Loulergue A case study on formal verification of the Anaxagoros hypervisor paging system with Frama-C

In International Workshop on Formal Methods for Industrial Critical Systems (FMICS 2015), LNCS, pages 15–30, Oslo, Norway, June 2015. Springer

Allan Blanchard, Nikolai Kosmatov, and Frédéric Loulergue A CHR-Based Solver for Weak Memory Behaviors

In Proceedings of the 7th Workshop on Constraint Solvers in Testing, Verification (CSTVA 2016), and Analysis co-located with The International Symposium on Software Testing and Analysis (ISSTA 2016), Saarbrücken, Germany, July 17th, 2016., pages 15–22, 2016

Allan Blanchard, Nikolai Kosmatov, Matthieu Lemerre, and Frédéric Loulergue Conc2Seq: A Frama-C Plugin for Verification of Parallel Compositions of C Programs In 16th IEEE International Working Conference on Source Code Analysis and Manipulation (SCAM 2016), 2-3 October 2016, Raleigh, NC USA, 2016

Program Verification

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Thank you for your attention !



Allan Blanchard, Nikolai Kosmatov, Matthieu Lemerre, and Frédéric Loulergue A case study on formal verification of the Anaxagoros hypervisor paging system with Frama-C

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Allan Blanchard, Nikolai Kosmatov, Matthieu Lemerre, and Frédéric Loulergue Conc2Seq: A Frama-C Plugin for Verification of Parallel Compositions of C Programs In 16th IEEE International Working Conference on Source Code Analysis and Manipulation (SCAM 2016), 2-3 October 2016, Raleigh, NC USA, 2016

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